

Each flip-flop-to-flip-flop path delay and a target machine cycle obtained in the stages of physical design and packaging design are used as input, and with respect to a path in which the path delay is not less than the target machine cycle, a closed loop including the path is extracted, and the timing of a clock signal of each flip-flop is adjusted so as to permit data transmission along the closed loop in a required cycle-number. At this time, a path along which data transmission is impossible in the target machine cycle or a closed loop including the path is listed in order to be modified. As methods of supplying a clock signal to each flip-flop, a plurality of methods different in the adjustable range of clock timing are combined and used.

Each flip-flop-to-flip-flop path delay and a target machine cycle obtained in the stages of physical design and packaging design are used as input, and with respect to a path in which the path delay is not less than the target machine cycle, a closed loop including the path is extracted, and the timing of a clock signal of each flip-flop is adjusted so as to permit data transmission along the closed loop in a required cycle-number. At this time, a path along which data transmission is impossible in the target machine cycle or a closed loop including the path is listed in order to be modified. As methods of supplying a clock signal to each flip-flop, a plurality of methods different in the adjustable range of clock timing are combined and used.